IDEC Chip Design Contest

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A Low-Power Wideband LNA with Inverter-Based Output Stage for Cryogenic Receiver

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Introduction

This circuit proposes a low-power wideband low-noise amplifier (LNA) with an inverter-based output stage, implemented in a Samsung 28-nm CMOS process for cryogenic receiver. As quantum computing systems scale, there is an increasing demand for high-performance receiver front-ends operating under strict cooling power constraints, making low power and low noise critical design goals. While conventional common-gate–common-source (CG–CS) LNAs provide wideband input matching, they suffer from relatively high power consumption for achieving sufficient gain. The proposed inverter-based output stage enhances effective transconductance and enables current reuse, improving gain efficiency and making it well suited for cryogenic operation.

Circuit Design

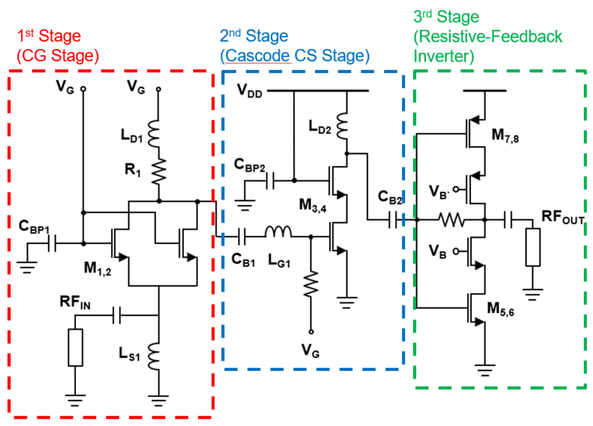

Fig. 1. Schematic of the proposed three-stage low-noise amplifier (LNA).

- **In wideband LNA design, the common-gate (CG) topology provides stable input matching over a broad frequency range without requiring complex matching networks, and is commonly combined with a common-source (CS) stage [1]. However, CG–CS structures require relatively high bias current to achieve sufficient gain, which becomes a critical limitation under the strict power constraints of cryogenic environments. In contrast, inverter-based amplifiers enable current reuse through simultaneous NMOS and PMOS operation, achieving higher effective transconductance under the same current [2]. Therefore, this work proposes a low-power wideband LNA that retains the advantages of the CG–CS structure while improving gain efficiency by incorporating an inverter-based output stage.**

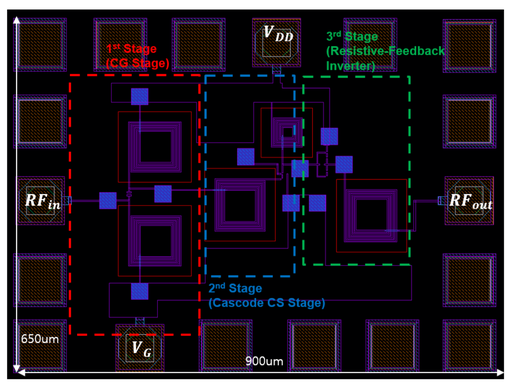

Fig. 2. Layout of the proposed low-noise amplifier (LNA).

- **The proposed LNA, shown in Fig. 1, is based on a CG–CS topology with an additional inverter-based amplification stage at the output. The common-gate (CG) input stage provides wideband input matching, while the common-source (CS) stage delivers the primary voltage gain. An inverter-based output stage is introduced to achieve additional gain without increasing power consumption. It is combined with resistive feedback or an appropriate load network to ensure stable operation, control output impedance, and improve frequency response flatness. The enhanced output gain also helps suppress the noise contribution from subsequent stages, improving overall receiver noise performance.**

Results

◆ Simulation Results

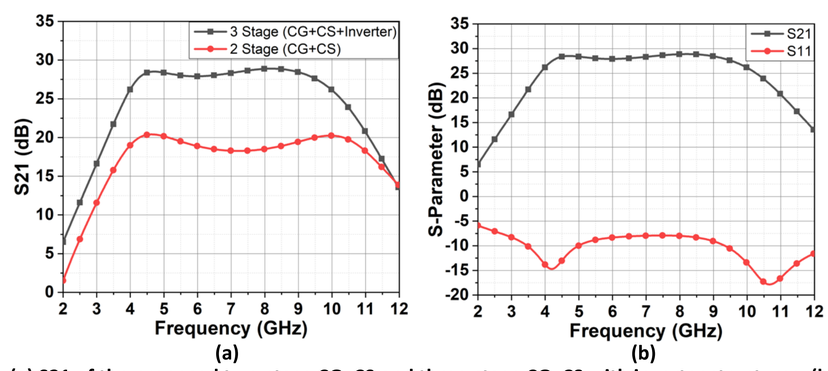

Fig. 3. (a) S21 of the proposed two-stage CG–CS and three-stage CG–CS with inverter structures. (b) S21 and S11 of the three-stage CG–CS with inverter structure.

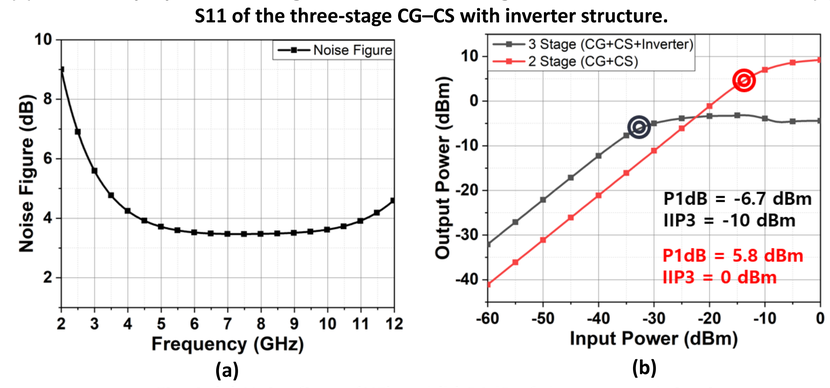

Fig. 4. (a) Noise figure (NF) and (b) P1dB of the proposed circuit.

◆ Comparison Table

	CS-CG	CG-CS+Inverter
Tech.	CMOS 28nm	CMOS 28nm
Frequency [GHz]	3.6-11	3.8-10.2
BW GHz]	7.5	6.4
S_{21} [dB]	18-20	28-29
S_{11} [dB]	< -8.5	< -8.6
NF [dB]	3.2-3.9	3.3-3.9
IP1dB [dBm]	-15.3	-33.7
OP1dB [dBm]	5.8	-6.7
IIP3 [dBm]	0	-10
Power Consumption [mW]	8.3	9.1
Area [mm^2]	0.16	0.22

[1] Y. -T. Lo and J. -F. Kiang, "Design of Wideband LNAs Using Parallel-to-Series Resonant Matching Network Between Common-Gate and Common-Source Stages," in IEEE Transactions on Microwave Theory and Techniques, vol. 59, no. 9, pp. 2285-2294, Sept. 2011.

[2] A. Caglar, S. Van Winckel, S. Brebels, P. Wambacq and J. Craninckx, "Design and Analysis of a 4.2 mW 4 K 6–8 GHz CMOS LNA for Superconducting Qubit Readout," in IEEE Journal of Solid-State Circuits, vol. 58, no. 6, pp. 1586-1596, June 2023.

This circuit proposes a low-power wideband low-noise amplifier (LNA) for cryogenic receiver applications, based on a CG–CS topology with an inverter-based output stage. Conventional CS–CG wideband LNAs provide stable input matching and broadband characteristics, but they require relatively large bias currents to achieve high gain, resulting in limited gain efficiency in terms of power consumption. To address this issue, this work introduces an inverter-based amplification stage at the output, increasing the effective transconductance under the same power conditions.